REMARKS

In the Office Action mailed February 8, 2005, claims 1-5, 8-10 and 12-22 are rejected under 35 U.S.C. §102(a) as being anticipated by Waizman (IEEE Feb. 1994). Claims 1, 2, and 4-11 are rejected under 35 U.S.C. §102(e) as being anticipated by Hassoun (U.S. Patent No. 6,487,648).

In response to the rejections, Applicants have amended independent claim 1 to indicate the actual clock signals generated at the outputs. In particular, Applicants have amended independent claim 1 to indicate that the digital clock manager comprises:

> "a delay lock loop (DLL) coupled to the reference input terminal, the skew input terminal, and the output terminal, wherein the delay lock loop generates an output clock signal at the output terminal; and
>
> a digital frequency synthesizer, having a variable oscillator, coupled to the delay lock loop and the frequency adjusted output terminal, wherein the digital frequency synthesizer generates a frequency adjusted clock signal at the frequency adjusted output terminal."

Applicants respectfully submit that neither Waizman nor Hassoun discloses or suggests the digital clock manager of claim 1. It is suggested in the Office Action that the delay lock loop of claim 1 is disclosed by the phase align circuit of Fig. 2 of Waizman, and that the output terminal is disclosed by "V_{CNTL}" in Fig. 2. However, Waizman discloses a DLL having a phase alignment circuit and a clock generator. As shown in Figs. 3 and 4, the phase alignment circuit generates a control voltage signal V_{CNTL} coupled to a clock generator, which comprises a voltage controlled delay line (VCDL). While the voltage control signal controls the delay value of the voltage controlled delay line, the voltage control signal is not a clock signal as claimed by Applicants. Further, Waizman fails to disclose or suggest a frequency adjusted output clock signal. Rather, Waizman merely discloses generating an output clock signal CLK which is a delayed version of the system clock XCLK. That is, the voltage controlled delay line generates a phase shifted output clock signal CLK having the same frequency as the system clock XCLK.

Similarly, Hassoun fails to disclose or suggest a digital frequency synthesizer having a variable oscillator which generates a frequency adjusted clock signal. It is suggested in the Office Action that the variable oscillator of claim 1 is disclosed in col. 11, lines 5-15 of Hassoun. However, the crystal oscillator described in col. 11, lines 5-15 generates the system clock "Clkp", and is not a part of the DLL 304A of Fig. 4. In contrast to the digital frequency synthesizer having a variable oscillator of claim 1, the crystal oscillator described in col. 11, lines 5-15 of Hassoun is not in the DLL 304A, which is cited for disclosing a digital frequency synthesizer. Further, Hassoun fails to disclose or suggest a digital frequency synthesizer which generates a frequency adjusted clock signal. That is, DLL 304A of Hassoun generates a phase shifted version of the reference clock. Applicants respectfully submit that claim 1 as amended and dependent claims 2-18 are allowable over the cited references, and respectfully request reconsideration of the claims.

In response to the rejection of independent claim 19 in view of Waizman, Applicants respectfully submit that the claim as pending distinguishes over Waizman. It is suggested in the Office Action that the V_{CNTL} signal of Waizman discloses a "synchronizing clock signal." However, as set forth above with respect to claim 1, V_{CNTL} is a voltage control signal which established a magnitude of a delay of the voltage controlled delay line, and not a clock signal as claimed by Applicants. Therefore, the output clock signal could not lag the synchronizing clock signal as claimed by Applicants in claim 9 if the voltage control signal is considered the synchronizing clock signal. Accordingly, Applicants respectfully submit that independent claim 19 and dependent claims 20-22 are not disclosed by Waizman, and respectfully request reconsideration of the claims.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 5, 2005.

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